REMARKS

In response to the rejections made on Claims 1-10 under U.S.C 102(b) as being anticipated by U.S Patent No. 6,147,530 Nogawa, the applicant has provided the following response:

The rejection of Claim 1 on Nogawa under 35 U.S.C. 102(b)

Regarding the rejection of Claim 1 on Nogawa (U.S Patent No. 6,147,530) under U.S.C.102(b), applicant has provided the following response:

Although Nogawa discloses a phase locked loop for generating a phase locked signal, and adjusting the frequency of the phase locked signal according to an incoming signal, applicant asserts that the disclosure of Nogawa and that of the present invention drastically differ in structure and methodology.

In particular, applicant asserts that the frequency detection module 260 of the present invention drastically differs from the frequency comparator 2 of Nogawa, in that the frequency comparator 2 of Nogawa clearly does not detect two regular patterns in an incoming signal as recited in the limitation of Claim 1 and otherwise suggested by the Examiner. To further clarify and define the limitation recited in Claim 1, the applicant has amended claim 1 to emphasize that fact that the incoming signal has periodic frames, and that the two regular patterns are detected between two different frames (one regular pattern in each of the two different frames constitute the two regular patterns). This amendment is fully supported in the original disclosure with no new subject matter added.

Operation of Nogawa' s frequency comparator 2 is explained and illustrated in Fig. 6, including the frame generating counter 25 (suggested by the Examiner for detecting the two regular patterns (the SYNC patterns) in the incoming signal through remarks for Claim 2). Nogawa states that the "frame generating counter 25 temporarily calculates one frame of the

EFM signal" (Col 13 lines 14-17), and that "At the head of the frame, a synchronization pattern (SYNC) exists" (Col 12 lines 61-62). Therefore, since the frame generating counter 25 of the frequency comparator 2 only calculates one frame, and each frame only contains only one SYNC pattern at the head of the frame, the frequency comparator 2 cannot detect two regular patterns (being the SYNC signals) in two different frames of the incoming signal, as recited in the limitation for amended claim 1 and otherwise suggested by the Examiner.

Furthermore, applicant asserts that the PLL of Nogawa simply detects any subsequent rising (or falling) edges in the incoming EFM signal. Because the nature of the EFM signal is arbitrary, mere detection of subsequent edges cannot be considered detection of a regularly repeating pattern. According to the disclosure of Nogawa, the "pulse width counting unit 21 detects rising and falling edges of data signal train ID using edge detecting circuit 211, measures the period of the detected edges by counter 212 with reference to regenerated clock CKI"(Col 13 lines 34-37). Therefore, the frequency comparator 2 utilizes the pulse width counting unit 21 to merely detect any rising or falling edge from in the data signal train ID. Since the signal train ID can be random or arbitrary in nature, applicant asserts that detection of subsequent edges in the signal pulse is not considered detection of two regularly repeating patterns.

This is in contrast to the present invention, where the frequency detection module 260 is indeed used to detect a regular pattern (being the SNYC patterns) in two different frames.

Additionally, since the PLL of Nogawa does not detect a regular pattern within two different frames of the incoming signal, applicant asserts that it cannot therefore calculate a number of periods of the phase locked signal corresponding to a distance between the two regular patterns through deductive reasoning. The recited limitation in claim 1 is as follows:

"a frequency detection module ... calculating a number of periods of the phase locked signal corresponding to a distance between the two regular patterns"

In summary, the PLL of Nogawa utilizes a method that determines the period between any subsequent rising or falling edges of an input signal, selects the period of shortest duration (Signal P3 in Fig 6), and uses the shortest period to determine the frequency discrepancy between the input signal and the phase generated signal to adjust the frequency of the PLL. This is in contrast to the present invention, which uses a method of counting the number of periods between two regularly repeating patterns in the incoming signal (the regular patterns appearing in two different frames), comparing the number of periods with a predetermined value (the number of expected periods in a frame) to determine a frequency discrepancy, and adjusting the frequency of the PLL based on the discrepancy.

The advantages offered by the present invention are readily apparent; it provides a method that averages the potential frequency variation over the course of at least one frame of the incoming signal by considering the total difference in periods between the two regular patterns and the expected value. The sampling window for counting the periods can also be enlarged beyond a single frame for a higher resolution. This technique is much better suited for cases where dynamic frequency shifts are applicable, as these variations can be averaged out over the time of the sampling window to help achieve a frequency lock. On the other hand, the PLL of Nogawa specifically considers a shortest period between subsequent edges of the input data signal to determine a synchronization discrepancy within a preset hold period. While this may provide a quicker reaction to an initial frequency discrepancy, for the case of dynamic frequency shifts, an overdamped response is anticipated before a steady state frequency lock is achieved.

For at least the structural and methodical differences of the frequency detection modules, applicant asserts that newly amended Claim 1 should be found allowable with respect to the teachings of Nogawa, and kindly requests that the Examiner consider allowance for amended Claim 1.

The rejection of Claim 2 on Nogawa under 35 U.S.C. 102(b)

Regarding the rejection of Claim 2 on Nogawa (U.S Patent No. 6,147,530) under U.S.C.102(b), applicant has provided the following response:

Applicant asserts that the composition of the frequency detection module 260 in the present invention differs significantly from the frequency comparator 2 of Nogawa (as otherwise suggested by the Examiner). A detailed description of the differences between the components and methodologies of these apparatuses are discussed further below.

Regarding the pattern detector, the Examiner has suggested that the frame generating counter 25 of Nogawa is also used to detect two regular patterns (identified as the SYNC patterns in EFM signal by Examiner) in the incoming signal. Applicant asserts that the frame generating counter 25 of Nogawa, is not however used to detect two regular patterns. As previously mentioned, the "frame generating counter 25 temporarily calculates one frame of the EFM signal... and supplies hold periods H1 and H2" (Col 13 lines 14-17), and "At the head of the frame, a synchronization pattern (SYNC) exists" (Col 12 lines 61-62). Therefore, since the frame generating counter 25 of Nogawa only calculates one frame, and each frame only contains one SYNC pattern at the head of the frame, it cannot detect the two regular patterns as two SYNC signals of the incoming signal as suggested by the Examiner. More specifically, the frame generating counter 25 of Nogawa is intended to supply hold periods H1 and H2 based on a single frame calculation. This is in contrast to the present invention, where the pattern detector is used to detect the two regular patterns (the SNYC patterns), such that the counter counts the number of periods N of the EFM_CLOCK signal between the two regular patterns.

Regarding the counter of the present invention, the Examiner suggests that the counter 212, and peak and bottom hold units 22 and 23 of Nogawa, are similarly for calculating the number of periods of the phase locked signal corresponding to the distance between two regular patterns (Examiner has identified the regular patterns as SYNC patterns). Applicant asserts that said components of Nogawa and the counter of the present invention are in fact

different and are utilized for measuring different quantities. Fig 6. from the disclosure of Nogawa illustrates that the Pulse width counting unit 21 comprises the edge detecting circuit 211 and a counter 212. According to the disclosure of Nogawa, the "pulse width counting unit 21 detects rising and falling edges of data signal train ID using edge detecting circuit 211, measures the period of the detected edges by counter 212 with reference to regenerated clock CKI"(Col 13 lines 34-37) and "counter 212 uses edge detection signal C1 and inverse regenerated clock CKI as a reset pulse and a clock respectively, and counts up at every period (T) of inverse regenerated clock CKI" (Col 13 lines 34-37). Applicant therefore asserts that the counter 212 of Nogawa does not measure the number of periods of the phase locked signal between the two regular SNYC patterns, rather, it measures the number of periods between any rising or falling edge from in the data signal train ID. As the data signal train ID is arbitrary, with it's digital data sequence determined specifically according to each manufacturer, applicant asserts that merely detecting any random subsequent edges in the data signal train ID cannot be considered detection of a regularly repeating pattern.

Regarding the comparator, the Examiner suggests that the frequency error output unit 24 of Nogawa accomplishes the same function of "comparing the number of periods with a predetermined value to generate a control signal, and using the control signal to control the oscillator to adjust the frequency of the phase locked signal" (Claim 2). In this case, the term "number of periods" refers specifically to the "number of periods of the phase locked signal corresponding to the distance between two regular patterns" as per Claim 2. From the previous remark regarding the counter, applicant asserts that the invention of Nogawa does not calculate the number of periods between two regular patterns, and as such, cannot compare this value using the comparator. More specifically, the "frequency error output unit 24 calculates the frequency difference between data signal train ID and inverse regenerated clock CKI based on the pulse width of bottom value P3" (Col 13 lines 9-12), where P3 (the value compared) is the shortest of peak values that refer to the period between any subsequent rising edges of the signal train ID (Col 13 lines 1-8). Because the comparator of the present

invention and the frequency error output unit of Nogawa compare two different quantities, applicant asserts that the two components are in fact different.

For at least the structural and methodical differences of the components above, applicant asserts that Claim 2 should be found allowable with respect to the teachings of Nogawa, and kindly requests that the Examiner reconsider allowance for Claim 2.

The rejection of Claims 3-6 on Nogawa under 35 U.S.C. 102(b)

Applicant kindly requests that Claims 3-6 be reconsidered in light of the response provided above for amended Claim 1. As Claims 3-6 are dependant on Claim 1, applicant asserts that if allowance is made for Claim 1, then similarly, allowances should be made for dependant claims 3-6.

The rejection of Claim 7 on Nogawa under 35 U.S.C. 102(b)

Applicant asserts that Claim 7 was rejected by the Examiner as being a method to operate the PLL based on the structure provided in previous Claim 1, also being rejected. In light of the amendment and response provided for Claim 1, applicant kindly requests that the Examiner re-evaluate Claim 7 and reconsider its allowance.

In particular, applicant asserts that step (b) (detecting two regular patterns in the incoming signal) of Claim 7 is not taught by Nogawa. In fact, the pulse width counting unit 21 of Nogawa "detects rising and falling edges of data signal train ID using edge detecting circuit 211, measures the period of the detected edges by counter 212 with reference to regenerated clock CKI"(Col 13 lines 34-37). As the data signal train ID is clearly arbitrary, applicant asserts that mere detection of any rising and falling edges from this signal does not merit detection of a regular pattern. Furthermore, without performing the method of step (b) in Claim 7, applicant asserts that subsequent steps cannot be performed through the teachings of Nogawa. For at least the above reasons, applicant kindly requests that the Examiner re-evaluate Claim 7 to consider its allowance.

The rejection of Claims 8-10 on Nogawa under 35 U.S.C. 102(b)

Applicant kindly requests that Claims 8-10 be reconsidered in light of the response provided above for Claim 7. As Claims 8-10 are dependant on Claim 7, applicant asserts that if allowance is made for Claim 7, then similarly, allowances should be made for dependant claims 8-10.

The introduction of Claim 11

Applicant has introduced Claim 11 in order to more accurately describe the PLL circuit of the present invention and further distinguish its architecture from the referenced PLL circuit of Nogawa.

Of particular note, a frequency detector and multiplexor are described. The multiplexor acts to select either the frequency detector or the frequency detection module to control the oscillator and adjust the frequency of the phase locked loop signal. The multiplexor also first selects the frequency detector to control the oscillator, and then selects the frequency detection module if the PLL has not entered into a locked state after a predetermined time. This configuration is not taught by Nogawa, as a single frequency comparator 2 (Fig. 2) is used to control the voltage controlled oscillator 5 regardless of whether a locked state has been achieved.

The limitations of Claim 11 are fully supported in the original disclosure, with no new matter being introduced.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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